Supplementary for

Calibration-Free Estimation Algorithm for Cuffless Continuous Blood Pressure Measurement based on ultrasonic devices

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Preparation process

The preparation of the ultrasonic array is divided into four parts: making the template, making the array, welding and packaging. For the template, we paste PI film on the aluminum plate, and then evenly cover a layer of Polydimethylsiloxane (PDMS) with a thickness of 400um on the PI mold and dry it, and then paste copper foil on the surface after drying. Then the required snake electrode is printed on its surface by laser printing method. To make the array, the excess copper foil on the template is removed first, and the solder paste or conductive silver paste is used as the adhesive. Piezoelectric particles are placed at the electrode and the adhesive is solidified by heating.

Drive system

The analog circuit of the drive system is required to achieve the functions of probe excitation and echo receiving, filtering and amplification, signal demodulation and phase orthogonal adjustment. First, the square wave signal is generated by FPGA development board (ALINX, ZYNQ7020), and the high-voltage digital pulse transmitter

(MAX4940) generates the excitation signal for the ultrasound array. Then the received echo signal from the ultrasonic array is amplified by the echo amplifier chip (AD8334) and then transmitted to the orthogonal demodulation chip (AD8339) to convert it into an IQ signal for complete output. Finally, this IQ signal is transmitted to the acquisition card (USB8584).

The high-voltage pulse driver module utilizes MAX4940 single chip technology to generate high-voltage, high-frequency unipolar or bipolar pulse output through low-voltage logic input control. The input EN can be used as an enable switch for four channels with each channel controlling positive and negative voltage outputs through three logic inputs CLP_, INN_, INP. Accurate control over FPGA output INN_ and INP_ delay allows precise management of high-voltage pulse phase.

The FPGA uses XC7Z020-2CLG400I model, Zynq7020 series and Xilinx chip. The on-board crystal oscillator provides 50 MHZ working clock. During operation, differential control signals INN_ and INP_ are outputted by FPGA to drive module while coarse delay is achieved by setting waveform of integer multiple periods. Fine delay is realized using a 185M clock counter for phase difference control along with synchronous clock and trigger signals at 10M HZ provided to acquisition module.

Furthermore, PLL IP core within FPGA provides a 100 times piezoceramics center frequency clock signal clk_out1 along with a 10MHZ acquisition card synchronous clock clk_out2.

The echo amplifier module utilizes the AD8334 integrated chip to control the echo gain. The channel is equipped with a built-in LNA, a VGA with a 48 dB gain range, and an optional gain post-amplifier with adjustable output limit function.

The LNA gain is 19 dB, which can realize single-ended input to differential output. A resistor can be used to adjust the LNA input impedance to match the signal source without affecting noise performance.

The gain of the post-amplifier can be selected to 3.5 dB or 15.5 dB by switching GN_HI_LO in order to optimize the gain range and output noise for 12 - or 10-bit converter applications.

The acquisition module uses the USB8584 data acquisition card of Altai Company. The data generated by the USB8584 will be temporarily stored on the onboard memory, and then transmitted to the system memory of the USB controller through the bus controller and USB interface for subsequent calculation and processing.

The USB8584 data acquisition card provides two acquisition methods: continuous sampling and finite point sampling. In multiple finite point sampling mode, the USB8584 can be used as an oscilloscope to observe the echo signal, and ensure that the array is attached to the appropriate position, and record the echo signal continuously with continuous or finite point sampling.

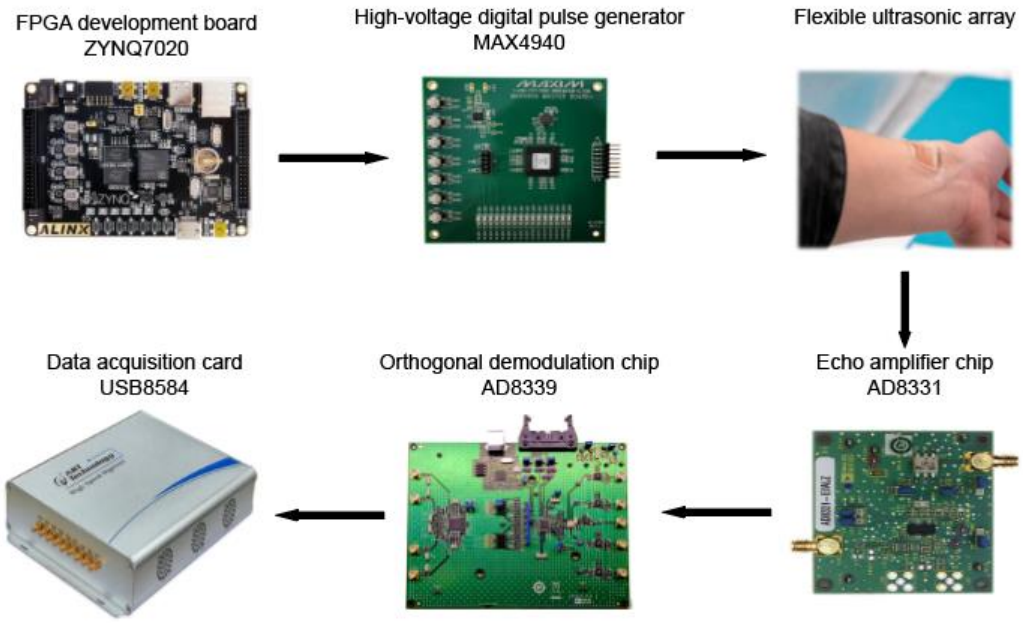

Fig.S1.

The driver system, including FPGA development board, High-voltage digital pulse transmitter, flexible ultrasonic array, echo amplifier chip, orthogonal demodulation chip and data acquisition card.

The effect of electrode arrangement

For the simulation of sound fields generated by piezoelectric particles, we conducted separate simulations for varying array numbers and spacings. The results indicate that:

(1) Larger spacing leads to a narrower main lobe width and more concentrated energy, but it also affects the maximum deflection angle.

(2) Increasing the number of array units results in a narrower main lobe width, more concentrated energy, improved directivity of the ultrasonic beam, and a pronounced focusing effect. However, this also increases system complexity and cost.

(3) A larger array size concentrates ultrasonic beam energy and narrows the main lobe width. Meanwhile, increasing array distance widens the array but also concentrates ultrasonic beam energy while producing more side lobes and gate lobes.

Ultimately, the ultrasonic array parameters we finally decided are: the ultrasonic frequency is 10 MHz, array size is 300um, array spacing is 100um, and array units is seven. The sound field simulation results are depicted in the figure below.

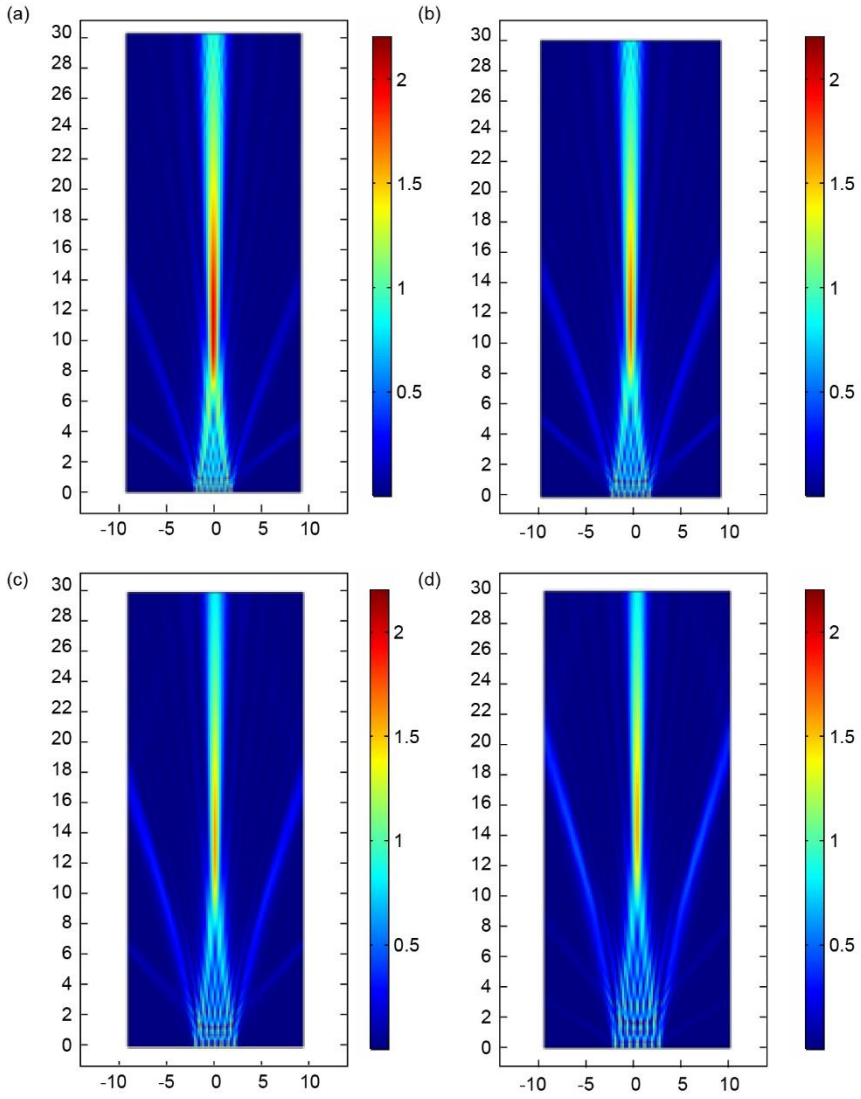

Fig. S2. Simulated focusing results with different array spacing. (a) When the array spacing is 75um, the main lobe width is the widest and the number of secondary lobes is the smallest. (b) When the array spacing is 100um, the main lobe width is small, and the number and amplitude of secondary lobes are well controlled. (c) When the array spacing is 125um, the main lobe width is narrow, but there is a large gate lobe. (d) When the array spacing is 150um, the main lobe width is narrower, and there is also a larger gate lobe.

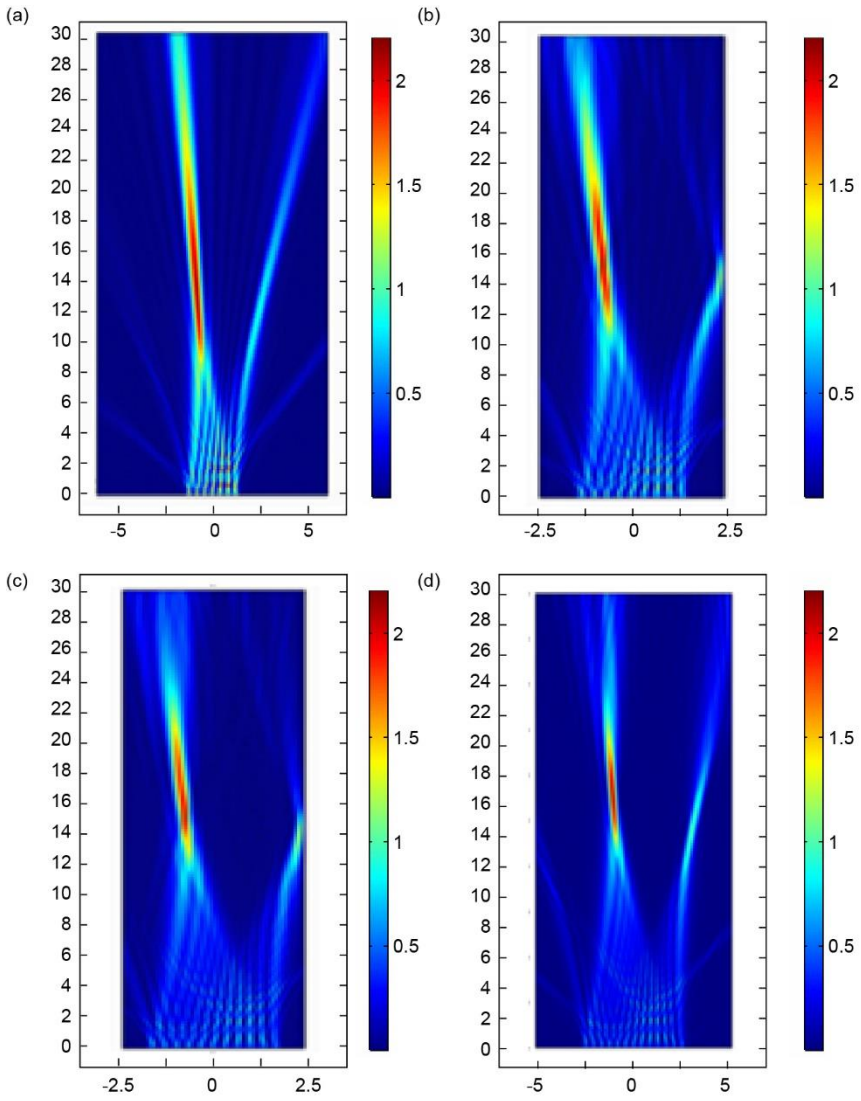

Fig. S3. Simulated focusing results with different array numbers. When the number of probe array elements increases, the width of the array elements will be larger, and the focusing effect will be improved, but the grating lobe and sidelobe will also increase. (a) Seven probes. (b) Nine probes. (c) Eleven probes. (d) Thirteen probes.